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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
MACKEY, TERRENCE M	

ART UNIT	PAPER NUMBER
1765	9

DATE MAILED: 06/05/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

mk-8

Office Action Summary	Application No.	Applicant(s)	
	10/034,483	PARKER ET AL.	
	Examiner	Art Unit	
	Terrence Mackey	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 61* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1 - 54 and 56* is/are allowed.

6)☒ Claim(s) *55 and 57 - 61* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Detailed Action

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 55, 57, 58, 60, and 61 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is unclear the relationship by which the etching of the second electrically-conductive stop layer provides exposed regions of the previously formed stop layer such that the subsequent step of forming an interconnect layer on the exposed regions of the previously formed etch stop may be performed.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 59 – 61 are rejected under 35 USC 102 (b) as being anticipated by Lee et al. (5,593,919).

Applicant claims a process for forming a high current, electromigration-resistant metal interconnect between circuit elements on a semiconductor substrate comprising the steps of providing a semiconductor substrate, forming a non-conducting layer thereon, planarizing the non-conducting layer, forming a circuit element layer overlying the non-conducting layer, forming an electrically-conductive stop layer overlying the circuit element storage layer, forming a hardmask overlying the stop layer, etching the hardmask layer to define an etch region, etching through the stop layer and the circuit element layer until the non-conducting layer is exposed using the etch region as an etch opening, forming an isolation layer extending over the hardmask layer and into the etch region, the isolation layer having sufficient thickness to fill in the gaps created by etching the etch region, planarizing the isolation layer until regions of the stop layer are exposed, and forming an interconnect layer over the exposed regions of the stop layer.

Lee et al. disclose a process for forming interconnects for a semiconductor device comprising steps for forming a first insulating layer over a semiconductor substrate, forming a first conductive layer over the first insulating layer, forming a first stopping layer over the first conductive layer, forming a second conductive layer over the first stopping layer, and patterning the firsts conductive, first stopping, and second conductive layers to remove the entire thicknesses thereof and expose the first insulating layer (column 4, lines 1-44). Lee et al. disclose that an additional layer of may be formed on top of the second conductive layer, the additional layer serving as an anti-reflective layer as well as being a polish stop layer (again see column 4, lines 1-44 and in particular lines 22-24 where it is disclosed that this additional layer may be

formed of TiN, SiN, Si-rich SiN, AlN, W, and the like). This additional layer is seen as serving as a hardmask in Lee et al.'s process. The patterning is performed using one or more steps with various types of different etch chemistries with the actual etch chemistry depending on the materials used for the various layers (column 4, lines 47-50). A second insulating layer is subsequently deposited to cover the patterned layers (shown as element 70 in Fig. 7) and polished to form a planar surface and remove portions of the second insulating layer that overlies the top surface of the second conductive layer.

Allowable Subject Matter

Claims 1 – 54 and 56 are allowed. The allowed claims are for a process of manufacturing an interconnect for a magnetoresistive memory on a semiconductor substrate comprising the steps of providing a semiconductor substrate, forming an initial dielectric layer thereon, planarizing the initial dielectric layer, forming a magnetoresistive storage layer overlying the initial dielectric layer, forming an electrically-conductive initial stop layer overlying the magnetoresistive storage layer, forming an electrically-conductive final stop layer overlying the initial stop layer, forming a hardmask overlying the final stop layer, etching the hardmask layer and the final stop layer until the initial stop layer is exposed to define an etch region, etching through the initial stop layer and the magnetoresistive storage layer until the initial dielectric layer is exposed using the etch region as an etch opening, forming an isolation layer extending over the hardmask layer and into the etch region, the isolation layer having sufficient thickness to fill in the

gaps created by etching the etch region, planarizing the isolation layer until regions of the final stop layer are exposed, and forming an interconnect layer over the exposed regions of the final stop layer.

The prior art, either singly or in combination, does not teach or fairly suggest applicant's claimed process for manufacturing an interconnect for a magnetoresistive memory array. It would not have been obvious to one of ordinary skill in the art at the time the invention was made to combine the cited prior art so as to arrive at the process taught by the applicant.

Conclusion

Remaining references cited to show the state of the prior art.

Claims 1 – 54 and 56 are allowed.

Papers relating to this application may be submitted to Technology Sector 1700 by facsimile transmission. Papers should be faxed to Crystal Plaza 3, Art Unit 1765, using fax number (703) 305-6357. All Technology Section 1700 fax machines are available to receive transmissions 24 hrs/day, 7 days/wk. Please note that the faxing of such papers must conform to the Notice published in the Official Gazette, 1096 OG 30, (November 15, 1989).

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Terrence Mackey whose telephone number is (703) 305-5504. The Examiner can normally be reached Monday - Friday from 7:00 AM – 4:30 PM.

If attempts to reach the Examiner by telephone are unsuccessful, the examiner's supervisor, Ben Uteck, can be reached at (703) 308-3836.